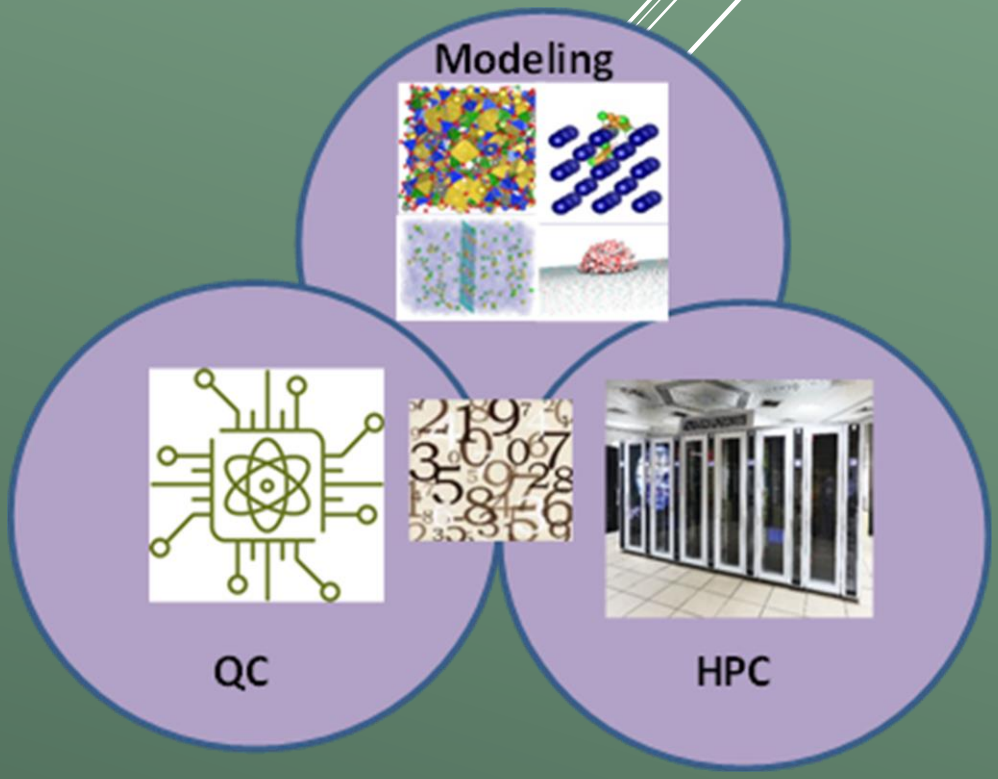
Proceedings of

DAE- BRNS National Workshop

"Parallel Computing in Science and Engineering (PCSE-2023)"

Wednesday, April 19, 2023



Venue:
Multipurpose Hall, TSH
Anushaktinagar, Mumbai

Organized By:
Chemical Engineering Division, Computer Division and Computational Analysis Division
Bhabha Atomic research Centre
Trombay, Mumbai – 400085

DAE- BRNS National Workshop

"Parallel Computing in Science and Engineering (PCSE-2023)"
Wednesday, April 19, 2023

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Scientific Programme

8:15-9:15	Registration of participants
	Inaugural Session
09:15	**Welcome Address by** Dr. S. Mukhopadhyay, Director, E&IG
	Address by Chief Guest Dr. Ajit Kumar Mohanty, Director, BARC
	Keynote address Title: **March from PetaFlops to ExaFlops: Challenges and Opportunities** Shri B S Jagadeesh, Technology Advisor, CDAC, Pune
	Vote of Thanks Dr. Sk. Musharaf Ali, Convener, PCSE-2023
	High Tea 10:30-10:50
11:00	*Keynote address* Title: **Towards Exascale Computing and Applications for DAE** Dr. S. Chaturvedi, Director, IPR, Gandhinagar
11:45	***Technical session I*** Title: **High Performance Computing Infrastructure for BARC** Shri K. Rajesh, Head CD, BARC, Mumbai
12:30	Title: **Advanced Supercomputer and its Applications** Shri N Sakthivel, CAD, BARC, Vizag
	Lunch Break 13:00-14:00
14:00	***Technical Session II*** Title: **Quantum information and computation - protection, control and encoding** Dr. Sudhir Jain, NPD, BARC, Mumbai
14:40	Title: **Large Scale Atomistic Modelling** Dr. Sk. Musharaf Ali, ChED, BARC, Mumbai
15:20	Title: **Parallel Computing Architectures and Parallel Programming Models** Shri Kislay Bhatt, CD, BARC
	Tea 16:00-16:15
16:20	***Technical Session III*** Title: **OpenMP and MPI based Parallel Programming** Shri K Vaibhav, CD, BARC
17:00	Title: **CUDA, OpenACC and OpenCL based Parallel Programming** Ms. Vibhuti Duggal, CD, BARC
17:45	***Conclusion Session***

Forwarded

We welcome you all to the National Workshop organized by Chemical Engineering Division, Computer Division and Computational Analysis Division, Bhabha Atomic Research Centre (BARC), Trombay, Mumbai, India. The Workshop is supported by the Board of Research in Nuclear Sciences (BRNS), Department of Atomic Energy (DAE) and is being held in multipurpose hall, TSH, Anushaktinagar. The computational capacity is growing rapidly with the continuing development of CPU and GPU based compute power as well as development of new and robust scientific and engineering software. Large scale computational modelling of molecules and materials and electromagnetics are crucial for addressing the technological challenges related to new generation of material and processes. The objective of the workshop is to bring together the experts in CPU and GPU based parallel computation, Quantum Computing and computational modelling in science and engineering from DAE and other research institutes to discuss the activities being pursued in the field of parallel computing and its application in atomistic and continuum modelling. This will help the users as well as the developers for effective utilization of immense power of advanced supercomputing facility available at their disposal. We sincerely thank all of them for their consent and timely submission of abstracts.

We are extremely grateful to Dr. A.K. Mohanty (Director, BARC) for his constant guidance, support and encouragement in organizing this workshop. We are extremely grateful to all the members of Advisory committee for their valuable guidance and support in formulating and shaping the workshop. The guidance, support and encouragement received from Shri S. Mukhopadhyay (Director, Electronics & Instrumentation Group and Chairman, Organizing Committee) and Shri K.T. Shenoy (Director, Chemical Engineering Group and Co-Chairman, Organizing Committee) during the entire process has been really gratifying and is being sincerely acknowledged. We are also grateful to Shri. Rajesh K. (Head, Computer Division), Dr. S. Mukhopadhyay (Head, Chemical Engineering Division) and Shri. U. D. Malshe (Head, Computational Analysis Division and Engineering Design & Development Division) for their suggestions and support in each step of the workshop.

About 100 delegates from DAE and non-DAE institutes are participating in this workshop. Total 10 invited lectures were received. This workshop will provide a platform for having close and fruitful interaction among various computational, experimental and theoretical research groups of DAE and other premier institutes of the country. This is expected to generate new ideas and will give the young researchers an opportunity to formulate their research in the frontier area of science and technology by leveraging the power of High Performance Computing.

For hosting this event, the Organizing Committee received help, support and encouragement from different quarters and we acknowledge all of them. We sincerely thank NR&ChEG Board and Trombay Council for giving consent to organize the PCSE-2023. We are grateful to all the organizing committee members for their efforts. We acknowledge the sustained support and cooperation extended by scientific/technical/non-technical staff of ChED, CD and CAD in organizing the workshop. We thank all the invited speakers, session chairpersons, faculty members, research scholars and students for their participations in this meeting. The Organizing Committee is grateful to Board of Research in Nuclear Sciences (BRNS) for financial assistance.

PCSE2023 Organizing Committee

डॉ. अजित कुमार मोहान्ती
Dr. Ajit Kumar Mohanty

भारत सरकार
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Member, Atomic Energy Commission

MESSAGE

I am delighted to know that a one day national workshop on "Parallel Computing in Science and Engineering" (PCSE-2023) is being organized in BARC, Mumbai on 19th April, 2023 at MPH, Training School Hostel, Anushaktinagar.

Parallel computing has revolutionized the way scientific and technological research is carried out in various fields of science and engineering. It has become an essential tool for running complex simulations, analysing massive datasets, and solving computationally intensive scientific problems. In BARC, "ANUPAM" project was conceived almost three decades ago with an objective to cater to the computational needs of diverse users and provide state of art infrastructure for high performance computing. Over the period of time, with latest technologies, processors, interconnect and indigenous designs, the computing ability has been scaled from few Megaflops to Petaflops meeting the requirements of general scientific computing, scientific visualization, information processing and diverse software applications involving atomistic and continuum modelling, electromagnetics, neutronics codes, life sciences and many more.

As the demand for increased computation shows no signs of slowing, it becomes apparent that there is a need to find ways to sustain increasing performance. To do so, the focus must be on improvements and innovations in parallel computing. This workshop is intended to encourage and enlighten the users about latest advancements in parallel computing and programming techniques for effective utilization of advanced supercomputing facility available in BARC and other DAE units.

In this workshop we have speakers from various DAE units, who are experts in the area of CPU and GPU accelerated parallel processing, quantum computing, atomistic modelling and parallel programming who will be sharing their knowledge and experience. I am sure the technical sessions will benefit the participants for developing their own software using advanced parallel programming techniques and tackle ever-more complex scientific problems in the fields of science and engineering. In the new era, in which parallelism is at the forefront, this is an opportune time for modernisation in programming systems and computing architectures. I hope the first-hand information from experts and interaction of the brightest minds of DAE and other premier institutes of the country will spark all of us to reach newer heights in the domain.

I would like to take this opportunity to complement all those involved in the organization of PCSE-2023 and wish the programme every success.

Ajit Kuma mohanty

Date : 18.04.2023

(Dr Ajit Kumar Mohanty)

March from Petaflops to Exaflops: Challenges and Opportunities

B.S. Jagadeesh
CDAC, Pune

In this talk, we propose to bring about the outcomes of the National Supercomputing Mission in the context of manufacturing Supercomputers entirely in the country beginning from designing, developing and deploying server boards to complete servers to interconnects to storage systems to Supercomputers along with representative applications of National Importance. Further, we will discuss about the Grand Challenge problems that require Exascale computing and huge opportunities that solving these would bring about for our country.

As of now, under National Supercomputing Mission, many Petaflop class of supercomputers have been designed and deployed at about Twenty Four Institutes (24) in the country. Leapfrogging to Exascale systems is indeed a challenge. We propose to bring about the challenges and opportunities in realizing Exascale systems entirely in the country. The talk explores the convergence of High Performance Computing and Artificial Intelligence domains and interesting architectures that may come out of this. Finally, we will have a look at the nice ecosystem of Semiconductor Industry, Electronic Manufacturing Services and the startup ecosystem that can bring in revolutionary changes in “Hardware Prowess” of India which aptly complements “our already established Software capabilities” to make us completely self-reliant and highly competitive.

Towards ExaScale Computing Facilities and Applications for DAE

Shashank Chaturvedi

IPR, Gandhinagar

Organisations under DAE undertake a wide range of activities, several of which require High Performance Computing (HPC). Over the past three decades, there has been a rapid increase in the HPC requirements of DAE, with a corresponding increase in the local HPC capacity set up by different organisations. Some of these organisations have also done path-breaking work in setting up HPC facilities using COTS components, in the parallelisation of in-house codes, and in developing new codes that are optimized for different environments, e.g. CPU/GPU. Some of the areas of work include CFD, PIC simulations for microwave sources/switches, MHD, Atomistic simulations (MD/MC), Bioscience applications, weather, AI/ML for voice/image/video/signal processing, thermal-hydraulics-neutronics, high-speed impact & shock waves, materials data generation under extreme conditions (e.g. EOS, opacity, resistivity, fracture properties), radiation damage, and so on. The HPC requirements of some of the Cis of HBNI have been assessed recently as part of a meeting organised by HBNI.

This talk will provide a glimpse of some of these simulations, a rough assessment of HPC requirements of DAE, and some suggestions on the way forward, including the possible development of quantum computing capability.

High Performance Computing Infrastructure for BARC

K. Rajesh

Computer Division

Bhabha Atomic Research Centre, Trombay, Mumbai

BARC is a premiere research organization working on the development, demonstration and deployment of technologies related to nuclear reactors, nuclear fuel cycle, isotopes and radiation applications. It carries out inter-disciplinary and multi-disciplinary R&D activities covering a wide range of disciplines in physical sciences, chemical sciences, biological sciences and engineering. Expertise at BARC covers the entire spectrum of science and technology. More than 4000 scientists and engineers working on various advanced R&D at BARC are extensively using computers for meeting their requirements of supercomputing, general scientific computing, scientific visualization, information processing and information exchange.

BARC has a mandate of providing centralized computing facilities for the scientists and engineers of BARC, a significant number of which work in fields that require access to high speed computers. The complex problems that these users attempt to tackle are such that they cannot be solved on conventional desktops or servers in a reasonable amount of time. The ANUPAM Supercomputer project has been fulfilling this ever-increasing demand for number crunching power for the last 3 decades.

This talk will cover the High Performance Computing Infrastructure made available to the scientists and engineers of BARC, viz. ANUPAM series of Supercomputers, Cloud Computing cluster, Machine Learning system and high throughput Mass Storage System.

Advanced Supercomputer and its Applications

N. Sakthivel
Computational Analysis Division
Bhabha Atomic Research Centre, Vizag

Scientific Computing at Exascale level has become a reality and the first ExaFlop Supercomputer is in operation. The Graphical Processing Units (GPU's) based architecture made it possible to reach ExaFlop level within the possible limits of power, cooling. The scientific applications development or porting of existing applications to utilize the accelerators has also evolved at a faster rate during the last few years.

This talk will present a glimpse of the growth of Supercomputers at the global level and its co-development for effective utilization of these advanced hardware for scientific applications.

Quantum information and computation - protection, control and encoding

Sudhir Jain

Nuclear Physics Division,

Bhabha Atomic Research Centre, Trombay, Mumbai

We shall discuss how quantum parallelism helps more efficient computation in certain complex problems. In this pursuit, an efficient way to correct errors becomes perhaps the most important subject of investigation. This is much more difficult in quantum computation as compared to classical computation. At the same time, lessons and ideas from classical computation are available. We shall discuss new ideas which have been shown to work in protection of qubits from noise, and, controlling quantum jumps. We also present a new quantum code which has the highest encoding rate hitherto achieved. Some results on molecular energies for simple molecules using quantum algorithms will be shown. We will conclude by showing a glimpse of (humble but definite) technological progress made by us in this area.

Large Scale Atomistic Modelling

Sk. Musharaf Ali
Chemical Engineering Division,
Bhabha Atomic Research Centre, Trombay, Mumbai
Homi Bhabha National Institute, Trombay, Mumbai

Development of new and novel molecules and materials for various applications in science and engineering by means of experiment alone is tedious and time consuming and costly affairs. Molecular engineering, encompassing density functional theory, molecular dynamics simulations and statistical mechanics are reasonably well established for understanding the molecular level phenomena and thus is central for guiding the difficult experiments like isotope separation of element and multi-component metal ions purification, sea water desalination and multi-component glass for immobilization of radionuclide and radiation shielding window. Molecular simulations are extensively used for physics based science discovery, drug design and bimolecular simulations.

The complexity of the molecular system depends on the nature of molecular system, type of properties and size of the molecular system. Atomistic simulations are commonly applied to understand the microscopic behaviors of the molecular systems and offer the macroscopic property which is experimentally observables. Atomistic simulations use mathematical approximations and computer programs to obtain results pertaining to chemical problems. Though small isolated molecule and liquid can be handled by desktop personal computers with low level computational methods, large molecular system and small molecular system with complex property cannot be treated with personal computer. This demands the requirement of large and fast computational power which can be extracted from the parallel computation. The present talk will discuss how the multiscale modeling results performed using parallel supercomputing facility can be utilized to interpret the experimental results and plan future experiments.

Parallel Computing Architectures and Parallel Programming Models

Kislay Bhatt
Computer Division
Bhabha Atomic Research Centre, Trombay, Mumbai

In this talk, there will discussion about modern Parallel Computing Architectures, which are being used today for expediting the computational tasks. The architectures like Symmetric Multiprocessor, Shared Memory, Massively Parallel, Cluster of Workstations and Accelerator based Heterogenous Architecture will be talked about. The usage of each type of architecture will also be discussed with example of each of the architectures and the types of jobs each architecture is suitable for.

Different types of Parallel Computing Architectures require different types of Programming Methodologies to encode Parallel Programs for them. There will be a discussion on various Parallel Programming Models, like Shared Memory Programming Model, Distributed Memory Programming Model, Data Parallel Programming Model and Programming Models for Heterogenous architectures. The usage of each type of Programming Model will also be discussed, i.e. which model is suitable for which type of problem or an application.

To execute a compute intensive task efficiently on a High Performance Computing (HPC) system, one needs to wisely choose an appropriate Parallel Computing Architecture and a compatible Parallel Programming Model depending on the type of parallelism and size of data involved in the problem he/she wants to attempt on the HPC system.

OpenMP and MPI based Parallel Programming

K. Vaibhav

Computer Division

Bhabha Atomic Research Centre, Trombay, Mumbai

Applications has to adopt to exploit the hardware prowess of the underlying system. Over a period of time with evolution of HPC applications standard APIs are defined to make the applications portable across the diverse hardware and architectures. These APIs abstracts the underlying communications layer and provide uniform deterministic over different platforms, allowing developer to focus more on application algorithms. Parallel computing is a type of computation in which problem in hand is divided in multiple sub tasks and processed simultaneously. Two most popular programming APIs are OpenMP and MPI.

OpenMP is an application programming interface that supports multi-platform Shared Memory multiprocessing programming in C, C++, and Fortran, on many platforms, instruction-set architectures and operating systems, including Solaris, AIX, FreeBSD, HP-UX, Linux, macOS, and Windows.

Message Passing Interface (MPI) is a standard, managed by MPI Forum, for applications running on distributed memory parallel computing architectures. The MPI standard defines the syntax and semantics of library routines that are useful to a wide range of users writing portable message-passing programs in C, C++, Python and Fortran. With MPI-2 and MPI-3 standards its coverage over the over the communication and inter process data exchange has vastly improved to make it most popular programming model for distributed architectures.

This talk will discuss about how to develop parallel applications using the above-mentioned APIs.

CUDA, OpenACC and OpenCL based Parallel Programming

Vibhuti Duggal

Computer Division

Bhabha Atomic Research Centre, Trombay, Mumbai

Heterogeneous computing is the well-orchestrated and coordinated effective use of a suite of diverse high-performance computing cores, such as CPU, GPU, DPU, VPU, FPGA, or ASIC to provide superspeed processing for computationally demanding tasks with diverse computing needs. The different elements are interconnected via high-throughput, low-latency channels so they can operate as a single unit.

CUDA is a parallel computing platform and programming model invented by NVIDIA. It can greatly improve computing performance by using the processing power of a graphics processing unit (GPU). CUDA is an extension of the popular C programming language, and programmers can use heterogeneous computing systems including CPUs and massively parallel NVIDIA GPUs.

OpenACC provides the ability to program using a familiar, high level programming model that provides both high performance and portability to a wide range of computing architectures. OpenACC uses high-level compiler directives to expose parallelism in the code and parallelizing compilers to build the code for a variety of parallel accelerators.

OpenCL is based on the C language standard and can provide cross-platform parallel computation APIs. OpenCL aims to develop portable parallel applications that execute across heterogeneous platforms consisting of central processing units, graphics processing units, digital signal processors, field-programmable gate arrays and other processors or hardware accelerators.

The talk will cover Heterogeneous programming using CUDA, OpenACC and OpenCL.

BOARD OF RESEARCH IN NUCLEAR SCIENCES

Board of Research in Nuclear Sciences (BRNS) supports research and development activity in universities, institutes of higher learning and national laboratories in India in the fields relevant to the mandate of Department of Atomic Energy. BRNS also supports symposia, conferences, seminars and workshops in various areas of science and technology.

Editorial

Sk. Musharaf Ali

Kislay Bhatt